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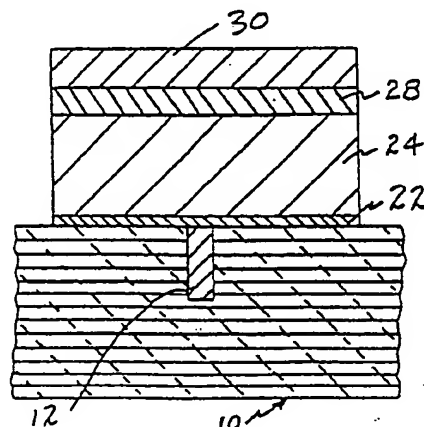
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(54) **Multilayered thin film metallurgy for brazing input/output pins to a ceramic substrate.**

(57) A multilayered thin film metallurgy for brazing input/output pins to a ceramic substrate is disclosed. A thin adhesion layer (22), which can suitably be a refractory metal such as titanium, vanadium, chromium or tantalum, is first formed on the surface of the substrate (10). A thick stress reducing layer (24) of soft metal such as copper, silver, nickel, aluminum, gold or iron is subsequently formed over the adhesion layer. To prevent the soft metal from reacting with subsequently brazed gold-tin pin eutectic alloy, a reaction barrier layer (28) which can be titanium or zirconium is then deposited over the soft stress reducing metal cushion layer. The process is completed by finally depositing a gold layer (30) over the reaction barrier layer.



**FIG. 2**

**EP 0 245 697 A2**

**MULTILAYERED THIN FILM METALLURGY FOR BRAZING INPUT/OUTPUT PINS TO A CERAMIC SUBSTRATE**

This invention relates to a multilayered thin film metallurgy for brazing input/output pins to a ceramic substrate.

The multilayer ceramic technology for integral mounting of semiconductor chips is well-known in the art. In semiconductor chip packaging, it is known to provide a ceramic substrate with termination pads on both the top and bottom surfaces of the substrate for attaching semiconductor chips, engineering change (EC) wires, input/output (I/O) connector pins, capacitors, etc. The assembled chip packages are then connected to the next level of packaging by means of the attached I/O pins on the bottom surface of the substrate.

The termination pads can be fabricated in a conventional manner by metal paste screening which upon sintering will become sintered dense metal pads suitable for the various interconnection purposes. Although this method of making termination pads has received wide acceptance in the alumina ceramic substrate technology, it nevertheless suffers from the disadvantage of requiring extreme care and attention when more fragile substrate materials such as glass ceramic are used.

Glass ceramics are known to have low dielectric constants and thermal coefficients of expansion (TCE) similar to silicon. For these reasons, it is desirable to use glass ceramics as a substitute for alumina ceramics in semiconductor chip packaging. Despite the desirability of employing glass ceramic in packaging technology, there is the problem of glass cracking due to the inherent fragile nature of the glass ceramic material. The thermal stresses experienced in the glass are principally due to the TCE mismatch between the I/O pad/pin joint and the glass ceramic substrate. It is further understood that the tensile stresses created along the radial direction in the immediate neighborhood of the I/O pad perimeters are critically dependent upon the following key factors: the size, thickness and geometry of the I/O pads; the material properties of the I/O pads; the pin joint morphology; and the distribution of braze alloy on the I/O pads.

It is therefore desirable to have a multilayered thin film metallurgy which can be tailored to minimize the internal stresses generated by the pin braze operation within the ceramic, yet also provide for adequate adhesion to the ceramic substrate.

The invention as claimed is intended to provide a multilayered thin film metallurgy for brazing I/O pins to a ceramic substrate and which includes a stress reducing cushion layer of soft metals which absorb the thermal as well as mechanical stresses from a brazed joint, thus significantly reducing the potential for cracking of the ceramic substrate.

In accordance with the invention a multilayered thin film metallurgy for brazing input/output pins to a ceramic substrate is disclosed. A thin adhesion layer, which can suitably be a refractory metal such as titanium, vanadium, chromium or tantalum, is first formed on the surface of the substrate. A thick stress reducing layer of soft metal such as copper, silver, nickel, aluminum, gold or iron is subsequently formed over the adhesion layer. To prevent the soft metal from reacting with subsequently brazed gold-tin pin eutectic alloy, a reaction barrier layer which can be titanium or zirconium is then deposited over the soft stress reducing metal cushion layer. The process is completed by finally depositing a gold layer over the reaction barrier layer. An additional layer of nickel or palladium may also be included between the titanium and gold layers for improved wettability, or a combined reaction barrier layer/Au layer phased region may be deposited to facilitate multiple reflow or repair cycles.

In the following the invention is described in detail with reference to the drawings wherein:

Fig. 1 is a cross-sectional view of a multilayer ceramic substrate.

Fig. 2 is a cross-sectional view of a 4-layer thin film structure in accordance with the present invention.

Fig. 3 is a cross-sectional view of a 5-layer thin film structure in accordance with the present invention.

Fig. 4 is a cross-sectional view of a 4-layer thin film structure with a reaction barrier/wettable surface phased region.

Referring to Fig. 1, the structural details of a preformed multilayer ceramic substrate 10 are illustrated. Ceramic substrate 10 includes a network of conductive vias 12 which terminate in input/output pads 14. Pads 14 can be used to provide connections for pins 16, engineering change wires 18, or other types of I/O connections. Semiconductor chip 20 also is connected to the top of the ceramic substrate 10. Referring to Fig. 2, the sequence of metallizing the I/O pad pattern begins with the alignment and attachment of a mask (not shown) to the ceramic substrate 10. The mask contains an image of the multilayer pad pattern to be depos-

ited. The type of mask used, metal, plastic, polymer, photoresist, etc. is not critical to this invention and can be any type commonly used in the art. Furthermore, the metallization pattern can be deposited in the desired pattern, or blanket layers of metal can be deposited over the entire substrate and then etched to form the desired pattern.

In the preferred embodiment, the formation of the multilayer thin film pads begins with the deposition of a thin layer of titanium 22 on the ceramic substrate 10. While titanium is the preferred adhesion layer, chromium, vanadium or tantalum can be used alternatively. The titanium layer 22 can be deposited by electron gun evaporation, sputtering, ion plating or other methods known in the art. The thickness of the adhesion layer 22 is preferably within the range 10 to 500 nm.

To promote the adhesion bonding between layer 22 and the substrate 10, the substrate temperature is maintained between 90°C and 350°C during evaporation.

A soft metal cushion layer 24 is next deposited over adhesion layer 22. Layer 24 serves primarily as a stress reducing cushion which absorbs and reduces the stresses transmitted from the pin joint 26 (Fig. 1) to the ceramic substrate 10, thus significantly reducing the ceramic cracking concerns. This observation is consistent with basic thin film theory which states that when a stress is applied to one side of a metal film, gradients of plastic strains (or stresses) will set up over distances determined by both the yield strength and the thickness of the film.

Typically, copper is used as the stress cushion material with the preferred thickness of approximately 6000 nm. However, thicknesses in the range 1000-20000 nm also demonstrated enhanced pin pull strength with reduced incidence of ceramic cracking. Other possible candidates for the soft metal cushion layer 24 include aluminum, gold, iron, nickel and silver. All of these materials have low yield strength and have demonstrated capability of absorbing high stresses from the pin joint.

To prevent the cushion layer 24 from reacting with the gold-tin braze alloy 26 (Fig. 1) used for joining pins 16, a reaction barrier layer 28 of titanium or zirconium is deposited over cushion layer 24. The thickness of the barrier layer 28 can range from approximately 200-1000 nm, depending on its reaction rate with the braze alloy. In the preferred embodiment, the reaction barrier layer 28 is approximately 500 nm thick. The use of higher volumes of Au-Sn braze at higher temperatures for a prolonged time would necessitate a thicker reaction barrier layer 28.

Other reaction barrier layer candidates include cobalt or nickel, although they would require a greater thickness, in the range 1500 to 3000 nm in order to protect the cushion layer 24 from reacting with the braze.

Finally, a wettable surface layer 30 is next applied over the barrier layer 28 to enhance the wettability of the multilayer film for pin brazing. Gold, approximately 500 nm in thickness, is preferred although the thickness can vary from 200-2000 nm.

Referring to Fig. 3, a thin layer of nickel or palladium 32, approximately 50-200 nm in thickness, may also be included between the reaction barrier layer 28 and wettable surface layer 30 for improved wettability.

In a modification to the multilayer structures previously described, after deposition of the reaction barrier layer 28, a thin layer 34, typically 100-500 nm, of Ti-Au or Ti-Cu phased region can be co-evaporated onto the pad, followed by a thin layer of gold 30 (Fig. 4). The compositions of Ti and Au or Cu can be controlled by simultaneously adjusting the deposition rates of the Ti and Au or Cu. With this blended structure, the phased layer 34 will maintain the slow reaction/dissolution rate with Au-Sn braze, and therefore will be capable of withstanding multiple chip reflow cycles without being completely reacted through. Furthermore, since Au or Cu is highly reactive with braze, blending them with Ti enhances the wettability of the reaction barrier layer.

This is especially beneficial to the pin repair operation since evidence has shown that repaired pins can wet more easily on pads which already have been reflowed repeatedly prior to the repair operation.

#### Claims

1. A multilayered thin film metallurgy for brazing input/output pins to a ceramic substrate (10) comprising:

an adhesion layer (22) deposited on said substrate;

a stress reducing layer (24) deposited over said adhesion layer;

a titanium barrier layer (28); and

a wettable surface (30) layer.

2. A multilayered thin film metallurgy on a ceramic substrate comprising:

an adhesion layer deposited on said substrate;

a stress reducing layer deposited over said adhesion layer;

a zirconium barrier layer; and

a wettable surface layer.

3. The multilayered thin film metallurgy as claimed in claim 1 or 2 wherein said adhesion layer is selected from the group consisting of titanium, vanadium, chromium or tantalum.

4. The multilayered thin film metallurgy as claimed in claim 1 or 2 wherein said stress reducing layer is selected from the group consisting of copper, iron, aluminum, silver, nickel, and gold.

5. The multilayered thin film metallurgy as claimed in claim 1 or 2 further including a layer of nickel (32) between said barrier layer and said wettable surface layer.

6. The multilayered thin film metallurgy as claimed in claim 1 or 2 further including a layer of palladium (32) between said barrier layer and said wettable surface layer.

7. The multilayered thin film metallurgy as claimed in claim 1 or 2 wherein said wettable surface layer is gold.

8. The multilayered thin film metallurgy as claimed in claim 4 further comprising a phased region (34) between the reaction barrier layer and the wettable surface layer comprised of a mixture of the reaction barrier layer and wettable surface layer.

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